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Clean Version of Pending Claims

ULTRA HIGH DENSITY FLASH MEMORY
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Serial No.: 09/866,938

Claims 62-76, as of January 30, 2003 (date response to first office action filed)

62. A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming first floating gate regions along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer;

forming first control gate regions between opposing first floating gate regions, the first control gate regions being separated from the first floating gate regions by a first intergate dielectric layer;

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

forming second floating gate regions along sidewall regions of the second troughs and separated from the sidewall regions by a second gate dielectric layer; and

forming second control gate regions between opposing second floating gate regions, the second control gate regions being separated from the second floating gate regions by a second intergate dielectric layer.

63. The method of claim 62, wherein the method further includes forming a first bottom insulation layer on bottom portions of the first troughs by thermal oxidation.

64. The method of claim 63, wherein the method further includes forming a second bottom insulation layer on bottom portions of the second troughs by thermal oxidation.

65. The method of claim 62, wherein the method further includes forming the second intergate dielectric layer by thermal growth of silicon dioxide.

66. The method of claim 62, wherein the method further includes forming the second intergate dielectric layer by deposition of oxynitride by chemical vapor deposition.

67. The method of claim 62, wherein the forming of the first source/drain layer includes forming the first source/drain layer at the surface of the substrate, wherein the substrate is a bulk semiconductor.

68. The method of claim 62, wherein the forming of the first floating gate regions includes forming the first floating gate regions along the sidewall regions of the first troughs and separated from the sidewall regions by the first gate dielectric layer, the first gate dielectric layer having an approximate thickness between 5 nanometers and 10 nanometers.

69. The method of claim 62, wherein the forming of the second floating gate regions includes forming the second floating gate regions along the sidewall regions of the second troughs and separated from the sidewall regions by the second gate dielectric layer, the second gate dielectric layer having an approximate thickness between 5 nanometers and 10 nanometers.

70. A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming a first gate dielectric layer along sidewall regions of the first troughs;

forming first floating gate regions along the sidewall regions of the first troughs and separated from the sidewall regions by the first gate dielectric layer, the first floating gate regions including a first conductive layer of N+ doped polysilicon;

forming first control gate regions between opposing first floating gate regions, the first control gate regions being separated from the first floating gate regions by a first intergate dielectric layer, and the first control gate regions including N+ doped polysilicon;

forming first gate lines in the first troughs between opposing first floating gate regions;

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

removing material at intersecting portions of first troughs and second troughs, thereby separating first floating gate regions into first isolated floating gates;

forming a second gate dielectric layer along sidewall regions of the second troughs;

forming second floating gate regions along the sidewall regions of the second troughs and separated from the sidewall regions by the second gate dielectric layer, the second floating gate regions including a second conductive layer of N+ doped polysilicon;

forming second control gate regions between opposing second floating gate regions, the second control gate regions being separated from the second floating gate regions by a second intergate dielectric layer, and the second control gate regions including N+ doped polysilicon; and

forming second gate lines in the second troughs between opposing second floating gate regions.

71. A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming first floating gate regions along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer, the first floating gate regions including a first conductive layer of N+ doped polysilicon;

forming first control gate regions between opposing first floating gate regions, the first control gate regions being separated from the first floating gate regions by a first intergate dielectric layer;

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

forming second floating gate regions along sidewall regions of the second troughs and separated from the sidewall regions by a second gate dielectric layer, the second floating gate regions including a second conductive layer of N+ doped polysilicon; and

forming second control gate regions between opposing second floating gate regions, the second control gate regions being separated from the second floating gate regions by a second intergate dielectric layer.

72. A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming first floating gate regions along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer;

forming first control gate regions between opposing first floating gate regions, the first control gate regions being separated from the first floating gate regions by a first intergate dielectric layer, and the first control gate regions including N+ doped polysilicon;

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

forming second floating gate regions along sidewall regions of the second troughs and separated from the sidewall regions by a second gate dielectric layer; and

forming second control gate regions between opposing second floating gate regions, the second control gate regions being separated from the second floating gate regions by a second intergate dielectric layer, and the second control gate regions including N+ doped polysilicon.

73. A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming first floating gate regions along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer;

forming first control gate regions between opposing first floating gate regions, the first control gate regions being separated from the first floating gate regions by a first intergate dielectric layer;

forming first gate lines in the first troughs between opposing first floating gate regions;

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

forming second floating gate regions along sidewall regions of the second troughs and separated from the sidewall regions by a second gate dielectric layer;

forming second control gate regions between opposing second floating gate regions, the second control gate regions being separated from the second floating gate regions by a second intergate dielectric layer; and

forming second gate lines in the second troughs between opposing second floating gate regions.

74. A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming first floating gate regions along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer;

forming first control gate regions between opposing first floating gate regions, the first control gate regions being separated from the first floating gate regions by a first intergate dielectric layer, and the first control gate regions are formed together with first gate lines by depositing N+ polysilicon in the first troughs;

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

forming second floating gate regions along sidewall regions of the second troughs and separated from the sidewall regions by a second gate dielectric layer; and

forming second control gate regions between opposing second floating gate regions, the second control gate regions being separated from the second floating gate regions by a second intergate dielectric layer, and the second control gate regions are formed together with second gate lines by depositing N+ polysilicon in the second troughs.

75. A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming first floating gate regions along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer;

forming first control gate regions between opposing first floating gate regions, the first control gate regions being separated from the first floating gate regions by a first intergate dielectric layer;

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

removing material at intersecting portions of first troughs and second troughs, thereby separating first floating gate regions into first isolated floating gates;

forming second floating gate regions along sidewall regions of the second troughs and separated from the sidewall regions by a second gate dielectric layer; and

forming second control gate regions between opposing second floating gate regions, the second control gate regions being separated from the second floating gate regions by a second intergate dielectric layer.

76. A method comprising:

forming a first source/drain layer at a surface of a substrate;

forming a second source/drain layer at a surface of an epitaxial layer;

etching, in a first direction, a plurality of substantially parallel first troughs in the epitaxial layer;

forming a first gate dielectric layer along sidewall regions of the first troughs;

forming first floating gate regions along the sidewall regions of the first troughs and separated from the sidewall regions by the first gate dielectric layer;

forming first control gate regions between opposing first floating gate regions, the first control gate regions being separated from the first floating gate regions by a first intergate dielectric layer;

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs in the epitaxial layer;

forming a second gate dielectric layer along sidewall regions of the second troughs;

forming second floating gate regions along the sidewall regions of the second troughs and separated from the sidewall regions by the second gate dielectric layer; and

forming second control gate regions between opposing second floating gate regions, the second control gate regions being separated from the second floating gate regions by a second intergate dielectric layer.